

REMARKS

Claims 6-21 have been allowed.

Claims 2-5 are objected to as being dependent on a rejected base claim. Applicants have amended claim 2 to include the limitations of base claim 1. Claims 2-5 are now in condition for favorable action and allowance.

Claim 1 was rejected under 35 U.S.C. 103(a) as being unpatentable over Fallah in view of Itakura.

Claim 1 has been amended to clarify the claimed invention and address antecedent issues. Applicants submit amended claim 1 distinguishes over Fallah and Itakura. Applicants claim compressing an n-bit binary signal for transmission over an m-bit bus (where $m < n$), and then decompressing the bus communicated signal to recover the original n-bit binary signal after transmission over the bus.

The Examiner primarily relies on Fallah. Fallah teaches a system and method for reducing transitions (i.e., switching activity) on a bus. This is accomplished through an address encoding technique which calculates an offset between a current address and prior address. A codeword is then created from the offset for communication over the bus. Importantly, Fallah does not teach reducing the number of bits communicated over the bus. This is shown in Fallah Figure 2 which illustrates that the input address has 32 bits, and the output signal on the bus also has 32 bits (B1-B32). Rather than reduce the number of bits on the bus, Fallah instead focuses on reducing the number of bit high/low and low/high transitions on the bus through the disclosed offset encoding technique. Absent a teaching in Fallah for the claimed reduction in number of bits for the bus communication, claim 1 distinguishes over the art.

CUSTOMER NO. 32914

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The secondary reference Itakura does not address the deficiencies of Fallah with respect to the claimed invention.

In view of the foregoing, Applicants respectfully submit that the application is in condition for favorable action and allowance.

Respectfully submitted,
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